We claim:

1. A pixel-capture circuit, comprising:

a pixel-capture device having a node and operable to convert light intensity into a pixel signal at the node, the pixel signal representing a captured pixel; and

a row node carrying a row signal that is operable to couple the node to a column trace during a read of the captured pixel and operable to set the node to a predetermined signal level during a reset phase.

2. The circuit of claim 1, further comprising a reset trace carrying a reset signal that is operable to uncouple the node from the row trace during the reading of the captured pixel.

3. The circuit of claim 2 wherein the pixel-capture device is disposed on a silicon substrate.

4. The circuit of claim 3 wherein the row trace, the column trace, and the reset trace are disposed within no more than two conductive layers disposed on the silicon substrate.

5. The circuit of claim 1 wherein the pixel-capture device comprises a photodiode.

6. The circuit of claim 1 wherein the pixel signal comprises a voltage.

7. The pixel-capture circuit of claim 1, further comprising:

a substrate;

two conductive layers disposed on the substrate; and

one or more conductive paths respectively operable to carry the row signal, each of the conductive paths disposed in a respective one of the two conductive layers.

8. The pixel-capture structure of claim 7 wherein the structure comprises no conductive layers disposed on the substrate other than the two conductive layers.

9. A pixel-capture circuit, comprising:

a pixel-capture device having a first and second node, the first node coupled to a first supply node;

a first transistor having a control node, a first drive node, and a second drive node, the control node coupled to the second node of the pixel-capture device and the first drive node coupled to a second supply node;

a second transistor having a control node, a first drive node, and a second drive node, the control node of the second transistor coupled to a row node, the first drive node of the second transistor coupled to the second drive node of the first transistor, the second drive node of the second transistor coupled to a column node; and

a third transistor having a control node, a first drive node, and a second drive node, the control node of the third transistor coupled to a reset node, the first drive node of the third transistor coupled to the row node, the second drive node of the third transistor coupled to the second node of the of the pixel-capture device.

10. The circuit of claim 9 wherein the first, second, and third transistors comprise MOSFET transistors.

11. A CMOS array comprising:

a plurality of pixel-capture circuits arranged in rows and columns, pixel-capture circuit comprising:

a pixel-capture device having a node and operable to convert light intensity into a pixel signal at the node, the pixel signal representing a captured pixel; and

a row node carrying a row signal that is operable to couple the node to a column trace during a read of the captured pixel and operable to set the node to a predetermined signal level during a reset phase.

12. The CMOS array of claim 11, further comprising a reset trace carrying a reset signal that is operable to uncouple the node from the row trace during the reading of the captured pixel.

13. The CMOS array of claim 12, further comprising a first conductive layer having the row trace and the reset trace disposed therein and a second conductive layer having the column trace disposed therein.

14. A system comprising:

a CMOS array having:

a plurality of pixel-capture circuits arranged in rows and columns, pixel-capture circuit comprising:

a pixel-capture device having a node and operable to convert light intensity into a pixel signal at the node, the pixel signal representing a captured pixel; and

a row node carrying a row signal that is operable to couple the node to a column trace during a read of the captured pixel and operable to set the node to a predetermined signal level during a reset phase; and

a processor coupled with the CMOS array and operable to facilitate the detection of a voltage signal at each column trace in each pixel in the CMOS array.

15. The system of claim 14, further comprising a memory coupled to the processor and operable to store the pixel signal.

16. A method, comprising:

integrating an amount of light;

generating a signal on a pixel node, the signal having a level related to the integrated amount of light;

reading the signal in response to a first control signal on a first control node; and

resetting the signal level at the pixel node in response to a second control signal on the first control node.

17. The method of claim 16, further reading the signal comprises detecting the level at a second control node.

18. The method of claim 16 wherein the resetting comprises:

setting the level at a third control node to a predetermined high level; and

pulsing the level at the first control node to a predetermined low level from a predetermined high level.